

ABSTRACT OF THE INVENTION

A memory includes an address bus, address counter, address decoder, comparator, and control circuit. During a data read or write cycle, the address bus receives an external address, the address counter generates an internal address, 5 which the address decoder decodes, and the comparator compares the external address to a value. Based on the relationship between the external address and the value, the comparator enables or disables the data transfer. For example, such a memory can terminate a page-mode read/write cycle by determining when the current external column address is no longer equal to the current internal column 10 address. This allows the system to terminate the cycle after a predetermined number of data transfers by setting the external column address to a value that does not equal the internal column address. Or, the comparator can compare the external or internal address to a predetermined end address, and the memory can terminate the cycle when the external or internal address equals the end address.

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